

INTERMODAL MATERIÉL
AND
NAUTICAL/NUCLEAR ANALYSIS
IMANNA
LABORATORY INC.

CERTIFICATION TEST REPORT

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TEST REPORT
16726-1
THERMAL EVALUATION
OF
PME MODULES
FOR
DNA GROUP

CUSTOMER:

DNA Group, Inc.
P.O. BOX 31727
RALEIGH, NC 27622

**MANUFACTURER
OF TEST ARTICLE:** DNA Group, Inc

REPORT NO.: 16726-1

IMANNA JOB NO.: 16726

CUSTOMER P.O. NO.: 550

DATE: Feb. 11, 2005

CONTRACT: N/A

PAGES IN REPORT: 13

STATE OF FLORIDA

ROBERT L. WHITE, being duly sworn, deposes and says: The information contained in this report is the result of complete and carefully conducted tests and is to the best of his knowledge true and correct in all respects.

Robert L. White

SUBSCRIBED and sworn to before me this 11th day of February, 2005

David H. Hudgins



David H. Hudgins
Commission # DD 010632
Expires May 3, 2008
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Imanna shall have no liability for damages of any kind to person or property, including special or consequential damages resulting from Imanna's providing the service covered by the report.

IMANNA LABORATORY, Inc.

TEST BY

Charles Herhold
PROJ. ENGINEER

1. TEST ARTICLE

Four Test Articles, each a representative sample of a solid state Power Management Enclosure (PME), were received for test. The devices were hermetically sealed in a manner typical of a production PME. However, the upper molded case cover of the test articles was of clear plastic to evaluate potential catastrophic damage to the PME circuit board. The test articles were submitted for test by the DNA Group, Inc. of Raleigh North Carolina.

2. MODEL NUMBER

Two PME units were identified as "GEN 1.0" and two PME units were identified as "GEN 1.8". For purposes of test and data recording, IMANNA marked the four units and monitored the temperatures on the components listed in Table One below.

TABLE ONE

<u>Device Label</u>	<u>Components monitored with individual thermocouples</u>		
GEN 1.0 #1	"uP" (microprocessor)	"U11" (a FET)	"U21" (a FET)
GEN 1.0 #2	"uP" (microprocessor)	"U11" (a FET)	"U21" (a FET)
GEN 1.8 #1	"uP" (microprocessor)	"TC1" (a FET)	"TC2" (a FET)
GEN 1.8 #2	"uP" (microprocessor)	"TC1" (a FET)	"TC2" (a FET)

3. REQUIREMENTS

The requirements for this effort are to perform a Thermal Evaluation of a PME while in elevated ambient temperatures and under various loads. The purpose of the thermal testing is to characterize how the solid state power management enclosures operate at higher ambient temperatures. The DNA Group's engineering team anticipates using this data to determine the maximum combined current the PME can handle as well as the maximum current capability of a FET under different ambient temperatures.

4. PROCEDURES

The testing will involve increasing the ambient temperature and then running a series of tests at the ambient temperature. Three thermocouples have been placed in each unit as indicated in the Table One above. DNA engineering reports that FET "U1" serves Pin 7 and FET "U21" serves Pin 37.

4.1 TEST SERIES ONE

This test is to determine the maximum allowed current for a FET, based upon the design of the PCB FET U14 which is connect to Pin 10 will have the worst thermal

characteristics.

This test will start with an ambient temperature of 20°C and then step up the current draw on pins 10 and 7 in selected increments, starting at 10 Amps and ending at 20Amps.

- 1) Set ambient temperature at 30°C.
- 2) Set current on pins 7 and 10 to 8 Amps.
- 3) Monitor temperatures, voltage and currents on pins 7 and 10.
- 4) If voltage or current drops note temperatures in report.
- 5) Wait till temperatures stabilizes or voltage/current drops on both pins, or one hour which ever comes first,
- 6) Increase current load on pins 7 and 10 by the predetermined level.
- 7) Repeat steps 3 - 6 till current is 18 Amps on pins 7 and 10.
- 8) Increase ambient temperature by 10°C
- 9) Repeat steps 2 - 8 with final test temperature of 70°C

4.2 TEST SERIES TWO

This test is to determine the maximum cumulative current consumption for the PME. That is at some point based on the total current the PME is sourcing and the ambient temperature the internal temperature of the microprocessors will exceed the maximum rating of 70°C.

This test will start with an ambient temperature of 20°C and increase ambient temperatures in 10°C increments with final test at 70°C. At each ambient temperature the cumulative load on the device will be increased in 10 Amp increments starting with 30Amps and ending with 70Amps. The GEN 1.0 and GEN 1.8 units require different loadings. Table Two below indicates the pin loading to use for each test.

- 1) Set ambient temperature at 30°C.
- 2) Apply 30 Amp load.
- 3) Wait till temperatures stabilize or one hour.
- 4) Record temperature, cumulative load and temperature.
- 5) Repeat steps 3 & 4 for next load in table.
- 6) Increase ambient 10°C.
- 7) Repeat steps 2-6 until 70°C is reached.

TABLE TWO

Cumulative (Amps)	Pin 1	Pin 7	Pin 10	Pin 31	Pin 34	Pin 37	Pin 40
30	5	5	0	0	0	10	10
40	5	5	5	5	0	10	10
50	5	5	5	10	5	10	10
60	5	10	5	10	5	15	10
70	5	10	10	10	10	15	10

Current consumption table for Gen 1.0

Cumulative (Amps)	Pin 1	Pin 2	Pin 37	Pin 31	Pin 33	Pin 30	Pin 40
30	5	5	0	0	0	10	10
40	5	5	5	5	0	10	10
50	5	5	5	10	5	10	10
60	5	10	5	10	5	15	10
70	5	10	10	10	10	15	10

Current consumption table for Gen 1.8

5. RESULTS SUMMARY

Thermal Evaluations each PME were performed while in elevated ambient temperatures and under various loads. The data will be used by DNA Group's engineering team to determine the maximum combined current the PME can handle as well as the maximum current capability of a FET under different ambient temperatures.

The results of the test are presented in the data sheets appended to this report. Photographs of the test articles, setup and loads are included. The test series was concatenated to obtain as much data as possible within the specified time and budget. Enough data was obtained to satisfy the needs of the DNA Group engineering team.

6. OBSERVATIONS AND COMMENTS

The results presented herein apply only to the test specimens as prepared and tested. All equipment used in the performance of these tests was calibrated to standards traceable to the N.I.S.T.

INSTRUMENTATION EQUIPMENT SHEET

Date: Jan 26, 2005 **Job No.:** 16726-1 **Customer:** DNA Group, Inc.
Technician: Herhold **Test Area:** Electrical Lab
Test Items: Four PME units

INSTRUMENT	MFG	MODEL	RANGE	ACCURACY	CAL DATE	CAL DUE
Temperature Chamber	Associated Testing Laboratories	SK 3105	-60°C to +150°C	+/- 1°C	Not Required	Not Required
Power Source (three)	Lambda Electronics	LFS-52-5-44147-4	Zero to 1,000Amps	0.1% Reg. 15mVoltrms Ripple	Not Required	Not Required
Computer 400MHz	John Key Corp.	AMD-K6	Multi.	Mfg.	Not Required	Not Required
Data Acquisition System	I/O Tech	DAQ Book 100	Multi.	0.1%	11-16-04	11-16-05
Data Acquisition Module	I/O Tech	DBK-19	T-Type T/C -200 +400°C	Res. (16bit) 0.1%	11-16-04	11-16-04
Clamp-On current Probe	ITT Instruments	MX 1200S	Zero to 1,000Amps	+/-1%	10-14-04	10-14-05

Instrumentation Information Verified by: *Alan Bell*

APPENDIX SUPPORTING DATA

TEST ONE
GEN 1.0 Unit #1

Chamber Temp Deg.C	Pin 7 Load Current Amps	Pin 10 Load Current Amps	Micro- Processor Temp Deg.C	U21 Temp Deg.C	U11 Temp Deg.C
30	0	0	30	30	30
30	10	10	52	78	76
30	13	13	54	82	107
30	15	15*	54	82	107
30	17	17*	55	82	136
30	18*	18*	55	81	137

40	0	0	40	40	40
40	10	10	61	85	84
40	13	13*	63	90	116
40	15*	15*	63	92	140
40	17*	17*	63	94	140
40	18*	18*	64	94	141

50	0	0	50	50	50
50	10	10	67	96	92
50	13	13*	71	102	127
50	15*	15*	72	104	142
50	17*	17*	72	104	141
50	18*	18*	72	104	141

60	0	0	60	60	60
60	10	10	74	104	101
60	13	13*	80	110	139
60	15*	15*	80	114	144
60	17*	17*	80	115	144
60	18*	18*	80	114	144

70	0	0	70	70	70
70	10	10	84	114	111
70	13	13*	88	121	150
70	15*	15*	88	123	147
70	NT-NDR	NT-NDR	NT-NDR	NT-NDR	NT-NDR
70	NT-NDR	NT-NDR	NT-NDR	NT-NDR	NT-NDR

* = Current flow is cycling OFF and back ON repetitively.

NT-NDR = No Test -- No Data Required

TEST ONE

GEN 1.0 Unit #2

Test Sequence abbreviated to collect key data.

Chamber Temp Deg.C	Pin 7 Load Current Amps	Pin 10 Load Current Amps	Micro- Processor Temp Deg.C	U21 Temp Deg.C	U11 Temp Deg.C
40	0	0	40	40	40
40	10	10	58	77	70
40	13	13#	62	81	98
40	15	15*	65	84	124
40	17*	17*	67	86	124
40	NT-NDR	NT-NDR	NT-NDR	NT-NDR	NT-NDR

50	0	0	50	50	50
50	10	10	68	91	81
50	13	13&	73	95	115
50	15&	15*	74	96	128
50	NT-NDR	NT-NDR	NT-NDR	NT-NDR	NT-NDR
50	NT-NDR	NT-NDR	NT-NDR	NT-NDR	NT-NDR

70	NT-NDR	NT-NDR	NT-NDR	NT-NDR	NT-NDR
70	NT-NDR	NT-NDR	NT-NDR	NT-NDR	NT-NDR
70	NT-NDR	NT-NDR	NT-NDR	NT-NDR	NT-NDR
70	NT-NDR	NT-NDR	NT-NDR	NT-NDR	NT-NDR
70	NT-NDR	NT-NDR	NT-NDR	NT-NDR	NT-NDR
70	NT-NDR	NT-NDR	NT-NDR	NT-NDR	NT-NDR

= Current flow is cycling OFF and back ON slowly,
rate is approximately 7Sec ON and 1 Sec OFF.

& = Current flow is cycling OFF and back ON slowly,
rate is approximately 4Sec ON and 1 Sec OFF.

* = Current flow is cycling OFF and back ON repetitively.

NT-NDR = No Test -- No Data Required

TEST ONE

GEN 1.8 Unit #1

Test Sequence abbreviated to collect key data.

Chamber Temp Deg.C	Pin 7 Load Current Amps	Pin 10 Load Current Amps	Micro- Processor Temp Deg.C	TC-1 Temp Deg.C	TC-2 Temp Deg.C
50	0	0	50	50	50
50	10#	0%	66	70	71
50	NT-NDR	NT-NDR	NT-NDR	NT-NDR	NT-NDR
50	NT-NDR	NT-NDR	NT-NDR	NT-NDR	NT-NDR
50	NT-NDR	NT-NDR	NT-NDR	NT-NDR	NT-NDR
50	NT-NDR	NT-NDR	NT-NDR	NT-NDR	NT-NDR
70	NT-NDR	NT-NDR	NT-NDR	NT-NDR	NT-NDR
70	NT-NDR	NT-NDR	NT-NDR	NT-NDR	NT-NDR
70	NT-NDR	NT-NDR	NT-NDR	NT-NDR	NT-NDR
70	NT-NDR	NT-NDR	NT-NDR	NT-NDR	NT-NDR
70	NT-NDR	NT-NDR	NT-NDR	NT-NDR	NT-NDR
70	NT-NDR	NT-NDR	NT-NDR	NT-NDR	NT-NDR

= Current flow is cycling OFF and back ON slowly,
rate is approximately 10Sec ON and 1 Sec OFF.

% = No current flow to Pin 10 as anticipated

NT-NDR = No Test -- No Data Required

TEST ONE

GEN 1.8 Unit #2

Test Sequence abbreviated to collect key data.

Chamber Temp Deg.C	Pin 7 Load Current Amps	Pin 10 Load Current Amps	Micro- Processor Temp Deg.C	TC-1 Temp Deg.C	TC-2 Temp Deg.C
50	0	0	50	50	50
50	10	0%	59	62	64
50	13*	0%	61	68	74
50	NT-NDR	NT-NDR	NT-NDR	NT-NDR	NT-NDR
50	NT-NDR	NT-NDR	NT-NDR	NT-NDR	NT-NDR
50	NT-NDR	NT-NDR	NT-NDR	NT-NDR	NT-NDR
70	NT-NDR	NT-NDR	NT-NDR	NT-NDR	NT-NDR
70	NT-NDR	NT-NDR	NT-NDR	NT-NDR	NT-NDR
70	NT-NDR	NT-NDR	NT-NDR	NT-NDR	NT-NDR
70	NT-NDR	NT-NDR	NT-NDR	NT-NDR	NT-NDR
70	NT-NDR	NT-NDR	NT-NDR	NT-NDR	NT-NDR
70	NT-NDR	NT-NDR	NT-NDR	NT-NDR	NT-NDR

* = Current flow is cycling OFF and back ON repetitively.

% = No current flow to Pin 10 as anticipated

NT-NDR = No Test -- No Data Required

TEST TWO GEN 1.0 Unit #1

Test Sequence abbreviated to collect key data.

Chamber	Pin	Pin	Pin	Pin	Pin	Pin	Pin	Pin	uP	U21	U11
Temp	Total	1	7	10	31	34	37	40	Temp	Temp	Temp
Deg.C	Amps	Amp	Amp	Amp	Amp	Amp	Amp	Amp	°C	°C	°C
50	0	0	0	0	0	0	0	0	NT	NT	NT
50	30	5	5	0	0	0	10	10	NT	NT	NT
50	40	5	5	5	5	0	10	10	NT	NT	NT
50	50	5	5	5	10	5	10	10	NT	NT	NT
50	60	5	10	5	10	5	15	10	NT	NT	NT
50	70	5	10	10	10	10	15	10	NT	NT	NT
70	0	0	0	0	0	0	0	0	NT	NT	NT
70	30	5	5	0	0	0	10	10	NT	NT	NT
70	40	5	5	5	5	0	10	10	NT	NT	NT
70	50	5	5	5	10	5	10	10	NT	NT	NT
70	60	5	10	5	10	5	15	10	NT	NT	NT
70	70	5	10	10	10	10	15	10	NT	NT	NT

NT = No Test

TEST TWO GEN 1.0 Unit #2

Test Sequence abbreviated to collect key data.

Chamber	Pin	Pin	Pin	Pin	Pin	Pin	Pin	Pin	uP	U21	U11
Temp	Total	1	7	10	31	34	37	40	Temp	Temp	Temp
Deg.C	Amps	Amp	Amp	Amp	Amp	Amp	Amp	Amp	°C	°C	°C
50	0	0	0	0	0	0	0	0	50	50	50
50	30	5	5	0	0	0	10	10	61	89	64
50	40	5	5	5	5	0	10	10	63	91	65
50	50	5	5	5	10	5	10	10	68	98	70
50	60	5	10	5	10	5	15	10	73	146	89
50	70	5	10	10	10	10	15	10	80	150	95
70	0	0	0	0	0	0	0	0	70	70	70
70	30	5	5	0	0	0	10	10	88	120	91
70	40	5	5	5	5	0	10	10	92	124	96
70	50	5	5	5	10	5	10	10	97	132	99
70	60	5	10	5	10	5	15	10	100	156	121
70	70	5	10	10	10	10	15	10	105	159	128

TEST TWO GEN 1.8 Unit #1

Test Sequence abbreviated to collect key data.

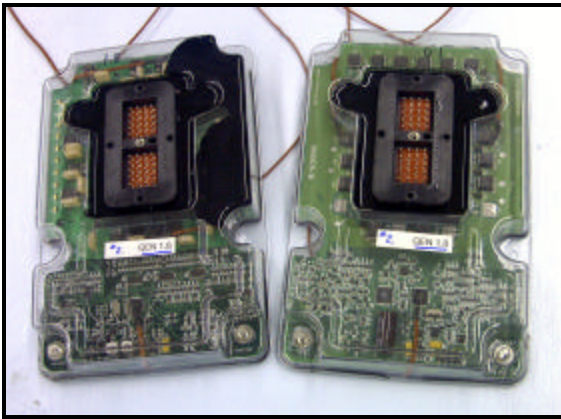
Chamber	Pin	Pin	Pin	Pin	Pin	Pin	Pin	Pin	uP	TC-1	TC-2
Temp	Total	1	2	37	31	33	30	40	Temp	Temp	Temp
Deg.C	Amps	Amp	Amp	Amp	Amp	Amp	Amp	Amp	°C	°C	°C
50	0	0	0	0	0	0	0	0	50	50	50
50	30	5	5	0	0	0	10	10	72	88	82
50	40	5	5	5	5	0	10	10	77	95	86
50	50	5	5	5	10	5	10	10	82	101	96
50	60	5	10	5	10	5	15	10	85	102	136
50	70	5	10	10	10	10	15	10	84	100	136
70	0	0	0	0	0	0	0	0	70	70	70
70	30	5	5	0	0	0	10	10	85	101	98
70	40	5	5	5	5	0	10	10	91	108	104
70	50	5	5	5	10	5	10	10	98	112	114
70	60	5	10	5	10	5	15	10	98	112	140
70	70	5	10	10	10	10	15	10	97	111	140

TEST TWO GEN 1.8 Unit #2

Test Sequence abbreviated to collect key data.

Chamber	Pin	Pin	Pin	Pin	Pin	Pin	Pin	Pin	uP	TC-1	TC-2
Temp	Total	1	2	37	31	33	30	40	Temp	Temp	Temp
Deg.C	Amps	Amp	Amp	Amp	Amp	Amp	Amp	Amp	°C	°C	°C
50	0	0	0	0	0	0	0	0	NT	NT	NT
50	30	5	5	0	0	0	10	10	NT	NT	NT
50	40	5	5	5	5	0	10	10	NT	NT	NT
50	50	5	5	5	10	5	10	10	NT	NT	NT
50	60	5	10	5	10	5	15	10	NT	NT	NT
50	70	5	10	10	10	10	15	10	NT	NT	NT
70	0	0	0	0	0	0	0	0	NT	NT	NT
70	30	5	5	0	0	0	10	10	NT	NT	NT
70	40	5	5	5	5	0	10	10	NT	NT	NT
70	50	5	5	5	10	5	10	10	NT	NT	NT
70	60	5	10	5	10	5	15	10	NT	NT	NT
70	70	5	10	10	10	10	15	10	NT	NT	NT

NT = No Test



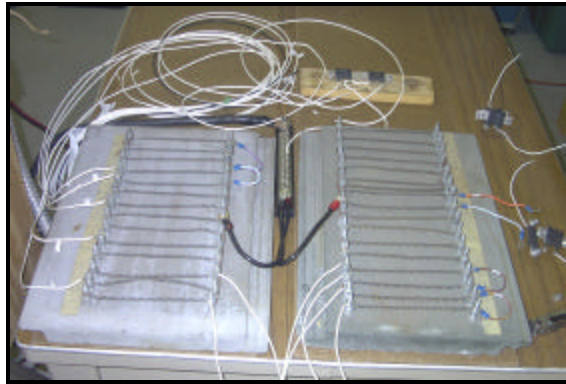
Test Articles as delivered, GEN 1.0 on right.



Typical test Article mounted in temperature chamber.



Current monitoring with clamp -on probe.



Resistive load array used for tests.



Overall view of test setup. Data acquisition unit position directly opposite temp. chamber's access port.